Avago HFCT-5951/5952 Single Mode Laser Small Form Factor Transceivers for ATM, SONET OC-12/SDH STM-4

Application Note 1275

Introduction

This document details the recommended circuit connections for Avago single mode LC Small Form Factor (SFF) OC-12 SONET/SDH transceivers.

Overview of HFCT-5951/5952

The HFCT-5951/5952 are high performance, cost effective modules for serial optical data communications applications specified for a signal rate of 622 Mb/s. They are designed to provide SONET/SDH compliant links for 622 Mb/s at both long and intermediate reach.

The modules are designed for single mode fiber and operate at a nominal wavelength of 1300 nm. They incorporate a high performance, reliable, long wavelength optical device and proven circuit technology to give long life and consistent service.

The transmitter section of the HFCT-595xATL/ATG/TL/TG incorporates a 1300 nm Fabry Perot (FP) laser. The transmitter in the HFCT-595xNL/NG uses a Distributed Feedback (DFB) Laser packaged in conjunction with an optical isolator for excellent back reflection performance. The transmitters are compliant to IEC 825 and CDRH Class 1 eye safety standards.

The receiver section uses a MOVPE grown planar SEDET PIN photodetector for low dark current and excellent responsivity.

A pseudo-ECL logic interface simplifies interface to external circuitry.

These transceivers are supplied in the new industry standard 2 x 10 and 2 x 5 DIP style packages with the LC fibre connector interface and are footprint compatible with SFF Multi Source Agreement (MSA).

Electrical Characteristics

Supply Voltage

The transceiver requires a positive power supply in the range of 3.14 V to 3.47 V. Care should be taken to avoid supply transients. These products are not recommended for 'hot-plug' applications.

Transmitter Section

Data Inputs

The Data and $\overline{\text{Data}}$ inputs should be ac coupled and 50 Ohm terminated externally. The transmitter inputs will accept standard PECL signals with levels ranging from 250 mV to 930 mV.

It is important to ensure data input lines have 50 Ohm characteristic impedance for optimum performance. Refer to 'Board Layout' Section for additional recommendations.

Single-ended operation is not recommended since data sheet specifications can only be guaranteed when both differential inputs are used. For input termination recommendations refer to the 'Termination schemes' section.

The laser is designed to operate with a 50% duty cycle or balanced signal, for normal operation. Failure to provide this may cause the optical parameters to move out of specification. Extinction Ratio and Duty Cycle Distortion may be affected. In the absence of data the module will emit a mean optical power within the specified limit.

Table 1. Avago single mode LC transceiver products

Part Number	+3.3 V	Intermediate Reach	Long Reach	2 x 5 Pinout	2 x 10 Pinout	–40 °C to +85 °C	0 °C to +70 °C	SD LVTTL
HFCT-5951ATL/ATG	✓	✓		✓		✓		✓
HFCT-5951NL/NG	✓		✓	✓			✓	✓
HFCT-5951TL/TG	✓	✓		✓			✓	✓
HFCT-5952ATL/ATG	✓	✓			✓	✓		✓
HFCT-5952NL/NG	✓		✓		✓		✓	✓
HFCT-5952TL/TG	✓	✓			✓		✓	✓

Optical Output

Figure 1 shows a typical HFCT-5951/5952 transmitter output waveform using the SONET OC-12 mask and optical filter.

Laser Bias Monitor

The laser bias monitor points (pins 17 and 18) allow the user to directly measure dc bias current (see Figure 2). The I/V relationship for laser bias current is:

I_{BIAS}= [(V18 - V17)/10] A

Note: When operating transceivers at low temperatures, the laser bias current is much reduced due to the low threshold of the laser. This may lead to low laser bias monitor voltages, see characterization report.

Note: The above relationship yields total laser forward current (threshold and bias) when no data is applied and approximately threshold current when modulation is applied. This monitoring facility allows the user to identify EOL conditions in a given application. *Figure 3* shows a circuit which can be used for indicating high bias current conditions. Pins 17 and 18 are connected to the inverting and non-inverting inputs of IC1A respectively. IC1A is configured as a unity gain buffer and its output (V_{IC1A}) fed to IC1B. IC2 provides a fixed 1.25 V reference to VR1 which allows fine adjustment for setting the threshold voltage (V_{TH}) at IC1B which is configured as a TTL comparator. The voltage V_{TH} at IC1B's inverting input determines the level at which the high bias conditions results in a TTL flag. For End of Life indication, a typical voltage setting for V_{TH} is:

- 3*(V_{IC1A} at +25°C, no input data modulation) for operation between +25°C – +70°C
- 1.5*(V_{IC1A} at +25°C, no input data modulation) for operation between 0°C – +25°C

These ratios are approximate and represent a coarse EOL indicator when used in conjunction with the circuit shown.

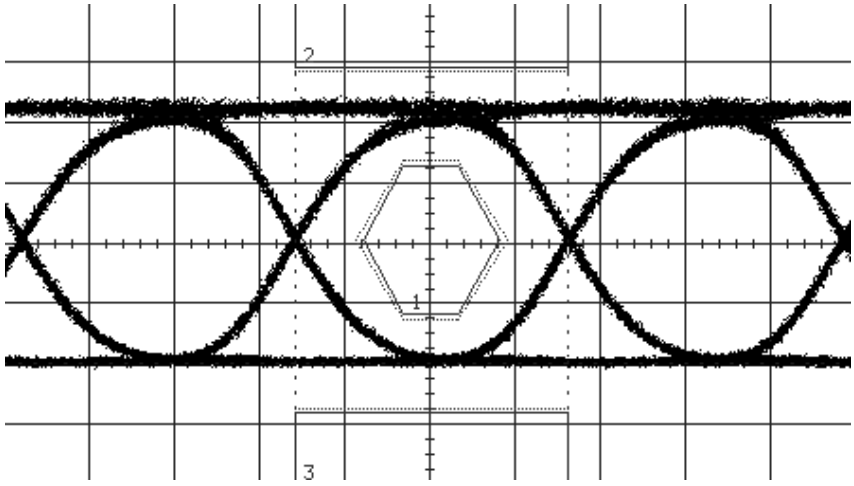


Figure 1. Typical HFCT-5951/5952 transmitter output showing OC-12 mask

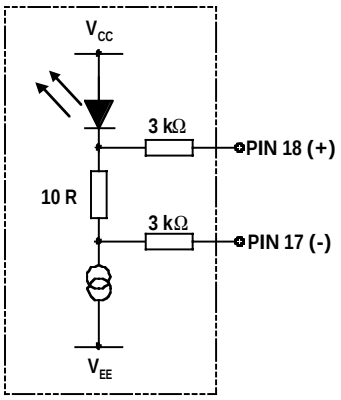


Figure 2. Bias monitor circuit

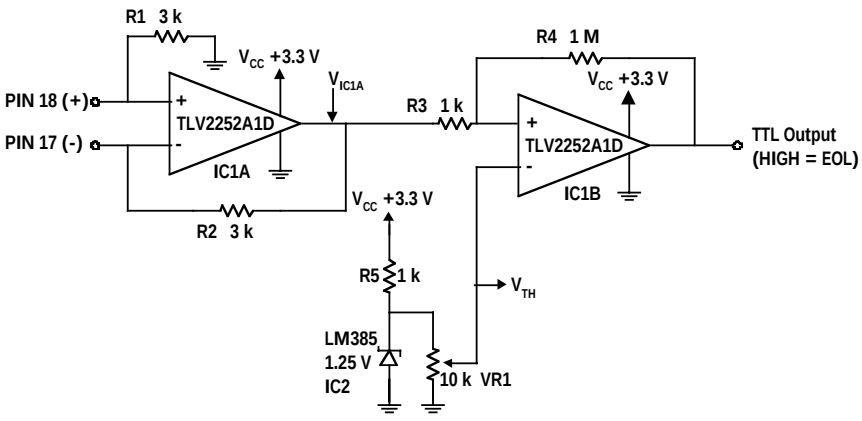


Figure 3. Laser bias indicator circuit

Rear Facet Monitor

The optical power rear facet monitor circuit provides a photo current which is proportional to the voltage measured between pins 19 and 20, this voltage is measured across an internal 200 Ω resistor (see Figure 4). **Note:** Any interconnecting circuit to these pins must have a high impedance input (>200 kW).

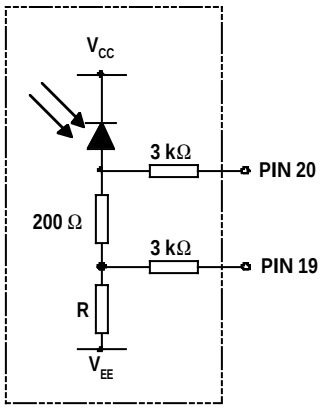


Figure 4. Rear facet monitor

Transmitter Disable

In normal operation (transmitter enabled) Pin 13 should be left open circuit (no external connection required). Connecting Pin 13 to V_{CCT} via a 500 Ohm resistor will disable the transmitter. This input pin is LVTTL compatible and requires a minimum of 50 µA for it to operate.

Transmitter Jitter Generation

The jitter generation requirements for SONET/SDH transport systems are:

- 100 mUI pk - pk (SONET)
- 10 mUI rms (SONET/SDH)

Typical jitter generation performance for the HFCT-5951/5952 is:

- 25 mUI pk - pk
- 2 mUI rms.

Figure 5 shows the experimental configuration used to test jitter generation. The transceiver is configured in electrical loopback. The optical O/P from an Omniber 377718A is used to provide a SONET STS12C, 2^{23}-1 PRBS scrambled pattern through an optical attentuator into the receiver of the DUT. The optical output of the transmitter is attenuated and fed into the OmniBER 37718A at an input sensitivity of –14 dBm. The receiver is independently optically stimulated with a SONET pattern to test for the effects of crosstalk.

Receiver Section

Data Outputs

Data and $\overline{\text{Data}}$ outputs are ac coupled and biased externally. Typical output swings are in the order of 700 mV. Figure 6 shows typical receiver waveforms.

It is recommended that the receiver outputs are connected to 50 Ohm differential transmission lines.

Signal Detect (SD)

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference. Pin 8 provides the SD function via a single-ended, dc coupled output and offers 3.3 V TTL capability. Interfacing this node to other stages requires a high impedance input typically in the order of 10 K Ohms. Low input impedance stages are unsuitable. This node may be left unconnected if not used. Hysteresis for the signal detect function is typically 1.7 dB.

The Signal Detect circuit provides a deasserted output signal when the optical link is broken or when the transmitter is OFF. The Signal Detect threshold is set to transition from a high to low state between the minimum receiver input optical power and –45 dBm avg. input optical power indicating a definite optical fault (e.g., unplugged connector for the receiver or transmitter, broken fiber, or failed far-end transmitter or data source). The Signal Detect does not detect receiver data error or error-rate. Data errors can be determined by signal processing offered by upstream PHY ICs.

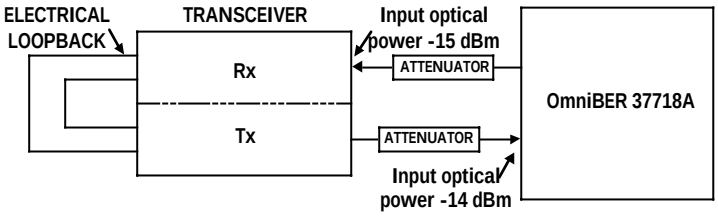


Figure 5. Jitter generation test configuration

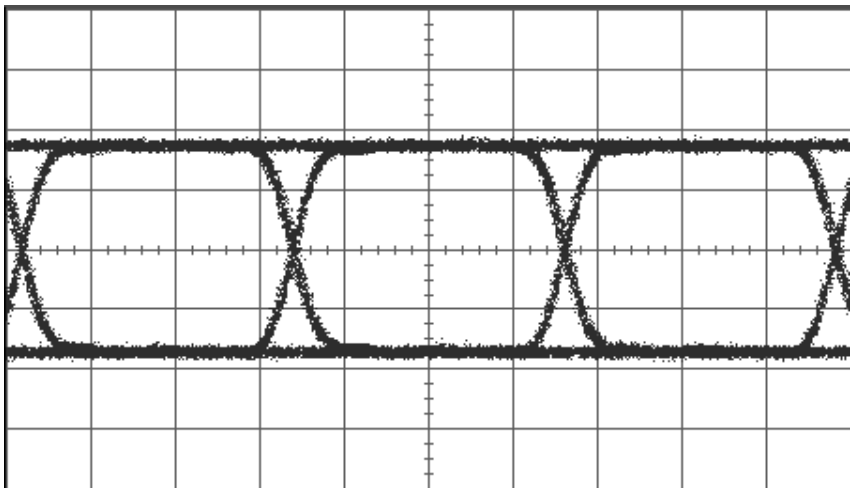


Figure 6. Shows typical receiver waveforms

PIN Photo Detector Bias Current Monitor

The designer also has the option of monitoring the PIN photo detector bias current. Figure 7 shows a resistor network, which could be used to do this. See *Figures 8a, 8b* and *8c* for alternative monitor ciruits for Pmon, Bmon and PDBias. It is essential to connect pin 1 to V_{CC}. If a bias resistor is used it should not exceed 200 Ω. Avago also recommends that a decoupling capacitor is used on this pin.

The typical responsivity of the photo detector bias monitor is shown in Figure 9. The bias current was measured using a pico ammeter in series with a 200 Ω resistor.

Optical Loopback

Note: When operating the HFCT-5952NL transceiver in optical loopback configuration, the overload limit of the receiver may be exceeded. Therefore, it is recommended that an optical attentuator should be used between the transmitter and receiver. (Typical overload for the HFCT-5952 is –1.5 dBm).

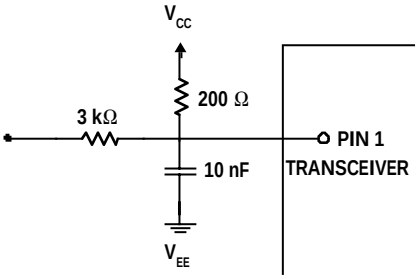


Figure 7. Recommended resistor network

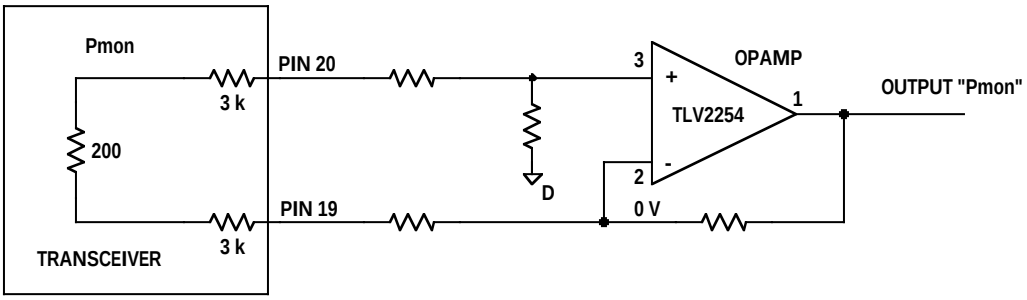
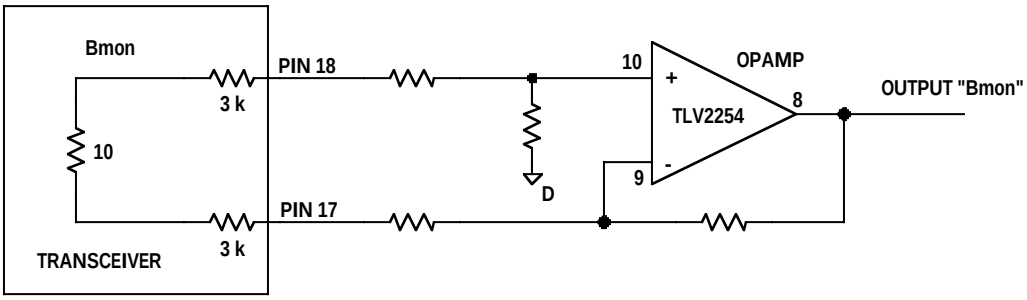


Figure 8a



NOTE: RESISTOR NETWORK SHOULD BE USED TO REFLECT THE GAIN REQUIRED BY THE INTERCONNECTING IC AND THE OUTPUT RANGE OF THE PRODUCT BEING USED. SEE CHARACTERIZATION REPORT.

Figure 8b.

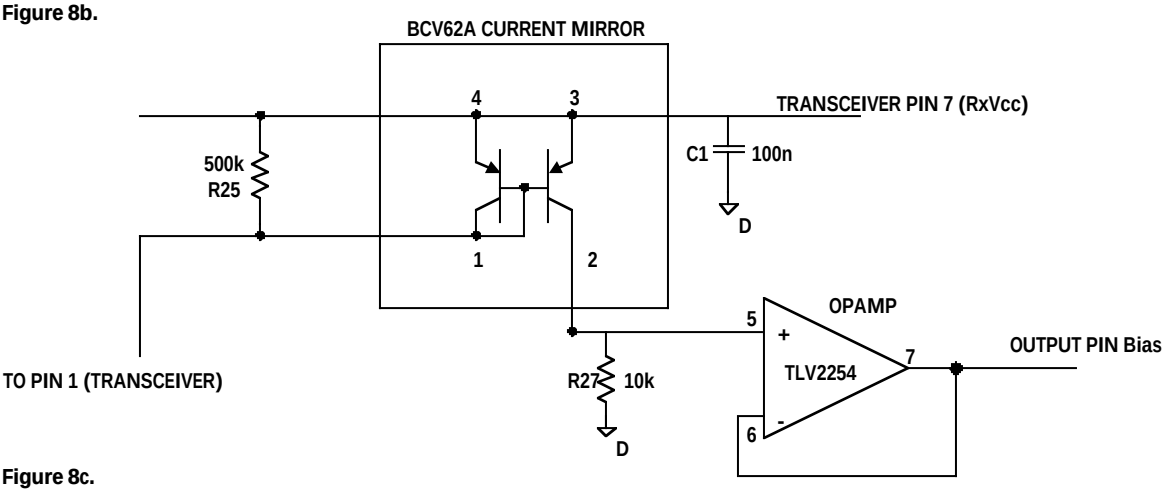


Figure 8c.

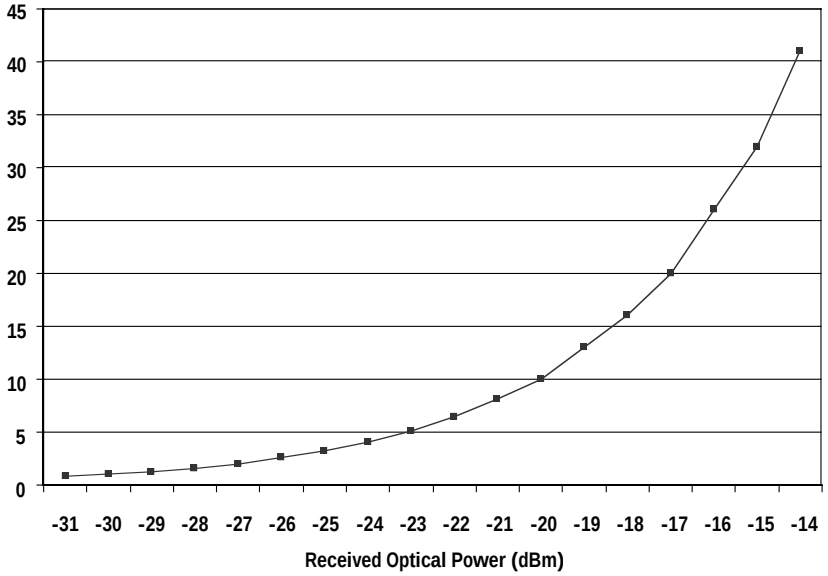


Figure 9. Typical responsivity of the photo detector bias monitor

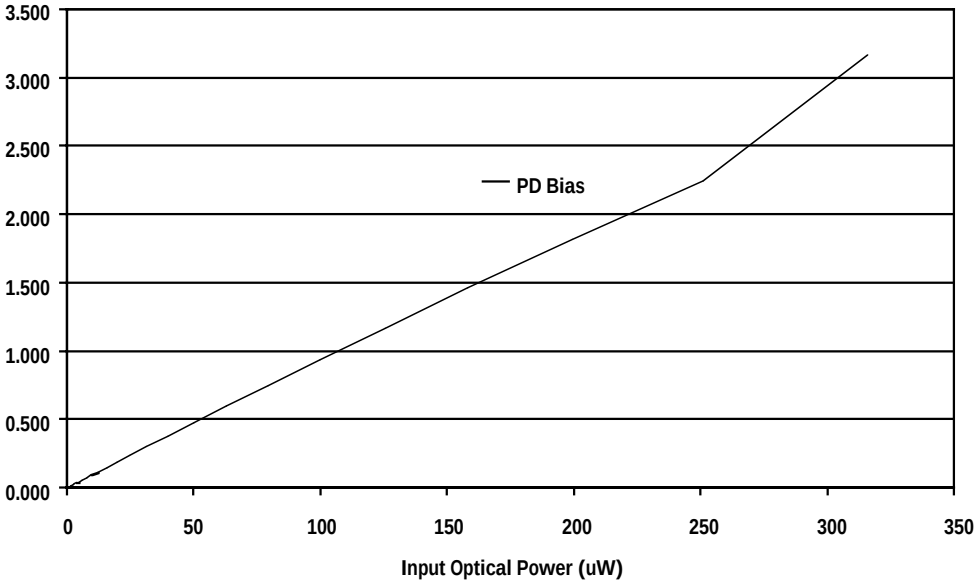


Figure 10. Typical results from plotting receiver input power vs PDBias output voltage using circuit in Figure 8c

Operating Wavelength

The HFCT-5951/5952 receivers are specified for operation over a range of wavelengths from 1270 nm to 1570 nm. *Figure 11* shows the typical dc responsivity curve of an InGaAs PIN Photodiode.

Power Supply filtering

Good power supply filtering is required for optimum performance. The LC filtering technique illustrated in the circuit diagram of *Figure 12* is recommended for the user. When using this filter arrangement, supply noise >100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, can be tolerated before a receiver sensitivity penalty of 1.0 dB occurs.

Power Dissipation and Thermal Analysis

Results for power dissipation and thermal analysis will be published when available.

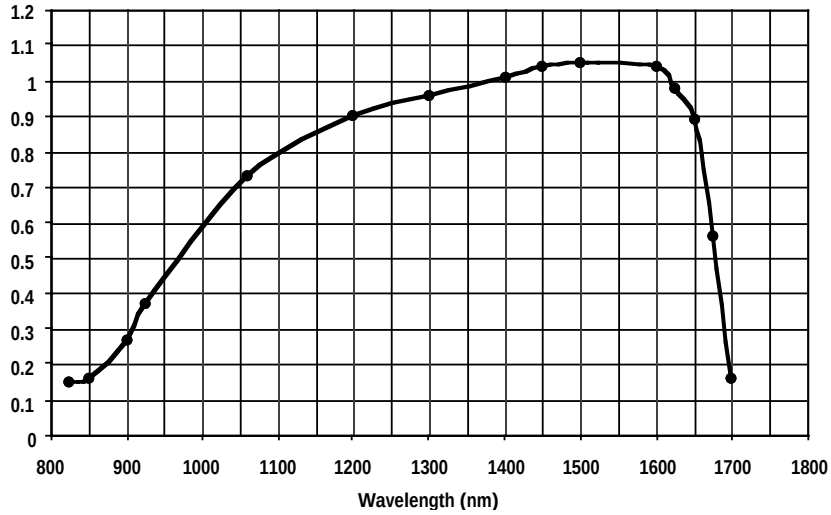


Figure 11. Typical dc responsivity graph of an InGaAs PIN photodiode

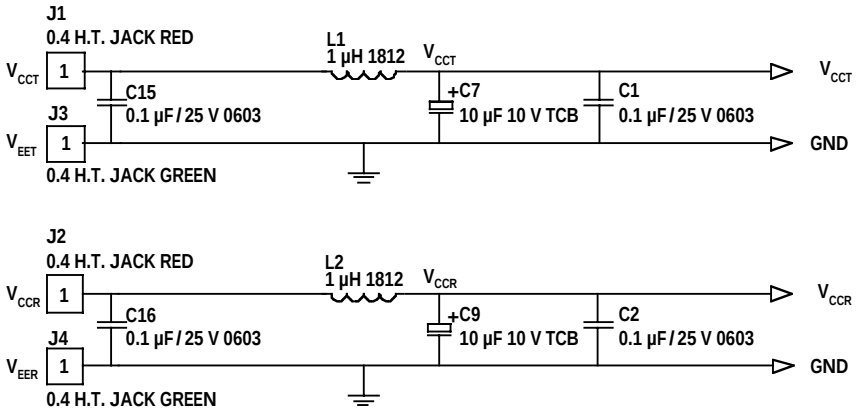


Figure12. Recommended filter

Evaluation Board

Description

The SFF test fixture, shown in *Figure 13,* has a four layer FR-4 printed circuit board with ground planes on both sides. It is designed to be footprint compatible for all 2 x 5 and 2 x 10 SFF variants. A weighted base enclosure is provided for stability on the bench. Edge-mounted SMA connectors are provided for data inputs and data outputs. Standard 2 mm sockets are included for easy connection to dc power supplies and monitors. A sliding switch is provided for selecting the transmitter disable function. Gold contact pin sockets are used to allow interchangeability between transceiver modules while assuring good connection integrity. The four grounding tabs and two mounting studs are all tied to the ground plane in the test fixture. However, under normal operation, it is recommended only the four grounding tabs to be connected to signal ground for optimum EMI compliance. The two mounting studs are either left floating or connected to chassis ground. Generous grounding is provided around the transceiver footprint using plated through holes.

Circuit Schematic

Figure 14 shows the circuit schematic for the test fixture. Separate power supplies are provided to the transmitter and receiver sections and recommended filtering arrangements are used. The Signal Detect (SD) function is provided for the user. This is single ended +3.3 V TTL output.

The photo detector bias (V_{pdR}) allows the monitoring of photo detector bias current through pin 1 of the 2 x 10 part. The pin should either be connected to V_{CCRX} directly or to V_{CCRX} through a resistor (R_2) for monitoring photo detector bias current which would be equivalent to $(V_{CC}–V_{PIN1})/R_2$.

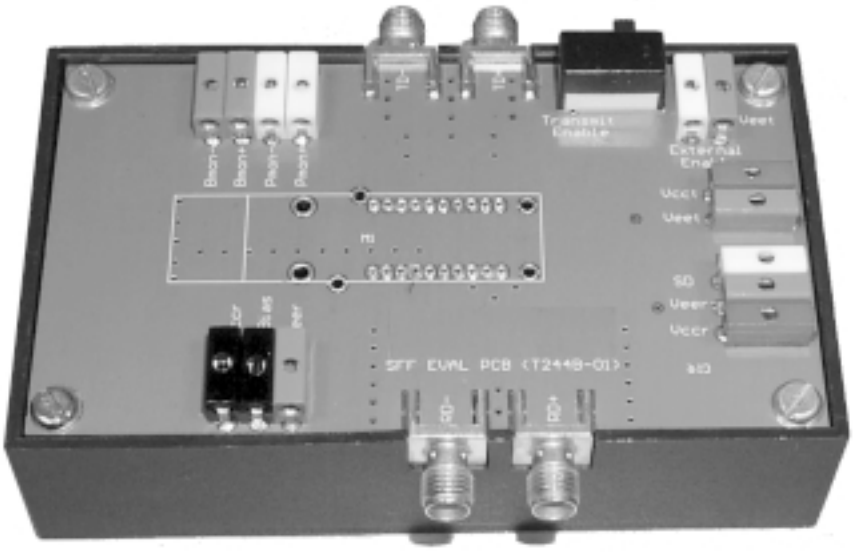


Figure 13. HFCT-595X Evaluation board

The laser diode bias current ($B_{MON+/–}$) is accessible by measuring the voltage across pins 17 and 18 of the 2 x 10 part. Dividing the voltage by 10 Ohm will yield the value of the laser bias current:

$I_{BIAS} = (V_{18}–V_{17})/10$ A

See Note on page 2.

It is worth noting that the above relationship yields total laser forward current (threshold and bias) when no data is applied and approximately threshold current when modulation is applied.

The back facet diode current monitor ($P_{MON+/–}$) is accessible by measuring the voltage across pins 19 and 20. Dividing the voltage by 200 Ohm will yield a value proportional to the photo current.

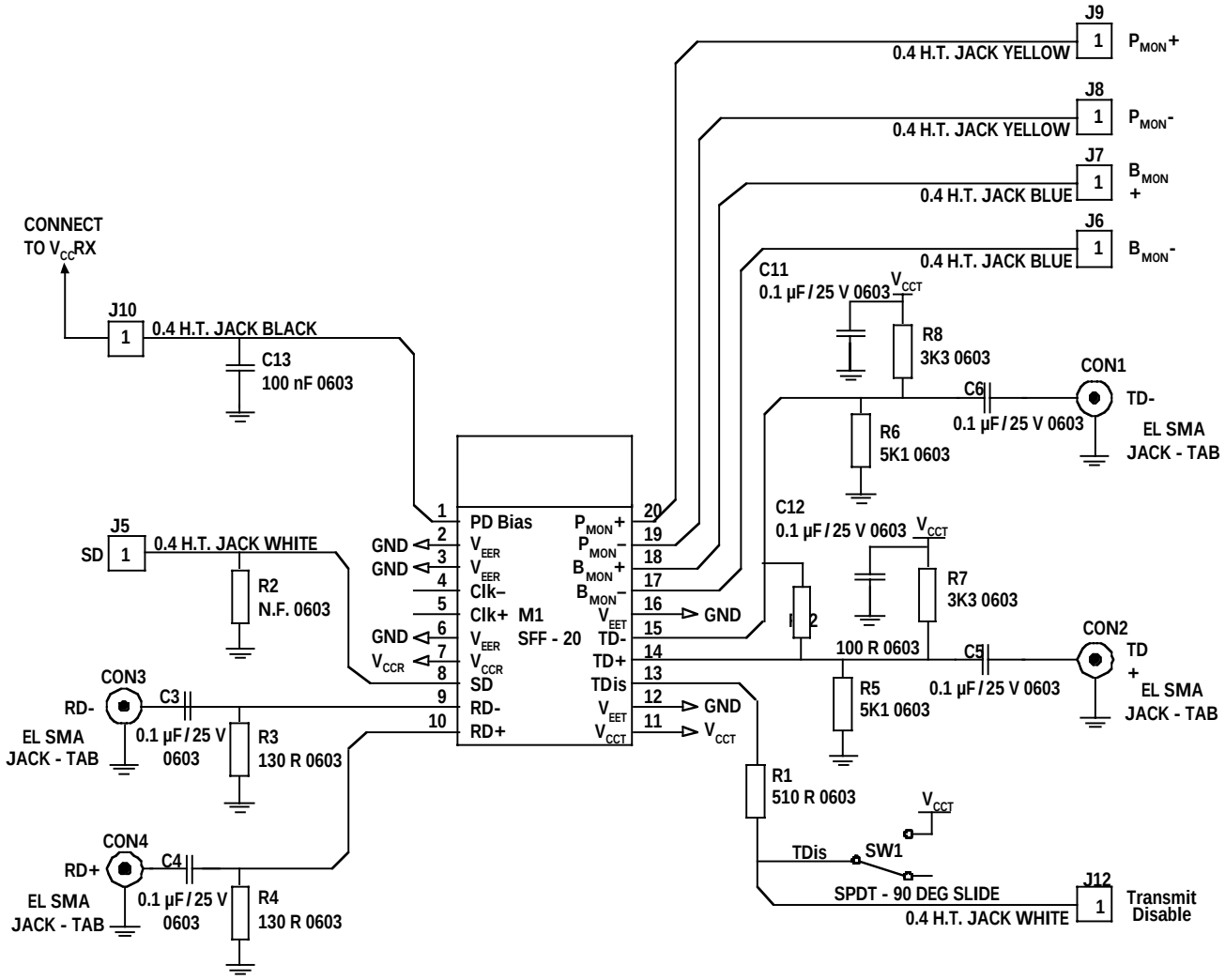
Figure 15 shows the power supply circuit fitted on the test fixture. Recommendations for optimum power supply noise reduction are currently under investigation. Results will be published when available.

Operation

The test fixture requires +3.3 V voltage supplies to both V_{CCT} and V_{CCR}. The Transmitter Enable/Disable switch needs to be in position 2 for normal operation while position 1 disables optical data transmission. The test fixture is rated for repeated temperature evaluation from –40°C to +85°C.

Optical Loopback

Note: When operating the HFCT-5951NL/5952NL (only) transceivers in optical loopback configuration, the overload limit of the receiver may be exceeded. Therefore, it is recommended that an optical attentuator should be used between the transmitter and receiver. (Typical overload for the HFCT-5951NL/5952NL is –1.5 dBm).



NOTE: ALTERNATIVE AC COUPLED CIRCUIT TO THAT RECOMMENDED IN THE DATA SHEET HAS BEEN USED. THIS CIRCUIT SEPARATES TRANSMISSION LINE TERMINATION AND INPUT BIAS NETWORK. TD± INPUTS ARE TERMINATED WITH 100 Ω LINE TO LINE RESISTOR. THE V_{CC}-1.3 V DC BIAS IS DEVELOPED VIA THE 3.3 kΩ / 5.1 kΩ NETWORK ON BOTH TD± INPUTS. TRANSMITTER POWER CONSUMPTION WILL BE REDUCED USING THIS CIRCUIT COMPARED TO THE COMMON 82 Ω / 130 Ω SCHEME.

Figure 14. SFF test fixture circuit diagram for 622 Mb/s transceivers

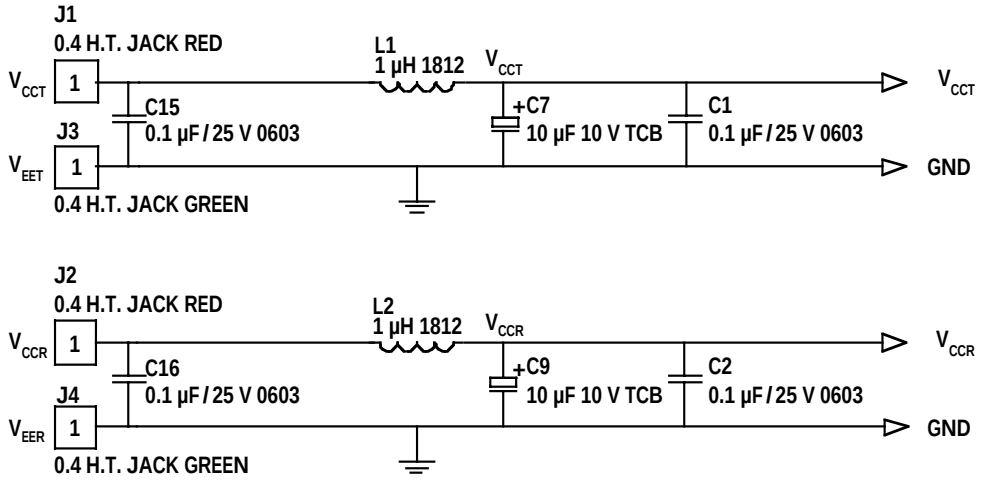


Figure 15. Filter network for power supply noise reduction

PCB Layout
Like all RF applications, the PCB design and layout for this high-speed transceiver requires careful consideration and attention towards interconnect impedance for DATA and CLOCK nodes. Any form of power supply filtering or decoupling should be done as close as possible to the power supply pins to minimize radiated or conductive pickup. It is recommended that high-speed data and clock tracks be buried striplines to minimize exposure of these lines for EMI suppression. Also, such an approach will ensure signal integrity and avoid waveform degradation from RF interference. Plated through holes or via used should be as small as possible to avoid impedance discontinuities along interconnecting tracks. Where ac coupling capacitors are required, small 0603 size components are recommended for minimizing variations in track impedance.

EMI Radiation/Susceptibility
One of a circuit board designer's foremost concerns is the control of electromagnetic emissions from electronic equipment. Success in controlling generated Electromagnetic Interference (EMI) enables the designer to pass a governmental agency's EMI regulatory standard and more importantly, it reduces the possibility of interference to neighboring equipment. Avago has designed the HFCT-5952 to provide excellent EMI performance. The EMI performance of a chassis is dependent on physical design and features which help improve EMI suppression. Avago encourages using standard RF suppression practices and avoiding poorly EMI-sealed enclosures.

Avago's OC-12 LC transceivers (HFCT-5951/5952) have nose shields which provide a convenient chassis connection to the nose of the transceiver. This nose shield improves system EMI performance by effectively closing off the LC aperture. Localized shielding is also improved by tying the four metal housing package-grounding tabs to signal ground on the PCB. Though not obvious by inspection, the nose shield and metal housing are electrically separated for customers who do not wish to directly tie chassis and signal grounds together. The recommended transceiver position, PCB layout and panel opening for both devices are the same, making them mechanically drop-in compatible. The recommended positioning of the transceivers with respect to the PCB and front panel is described in the Data Sheet.

Recommendation for mounting studs and grounding tabs EMI and susceptibility results to be published when available.

Compatibility Trials
The HFCT-5951/5952 transceivers have been evaluated using AMCC Mux/Demux chipsets and compatibility has been confirmed. The aim of this exercise was to design functional boards with a view of sharing relevant layout and circuit information with the optics system designer. Full description of the design, layout, measurements and results are beyond the scope of this document but a separate document is available. Please contact your Avago representative for further information.

Recommendations for 2 x 5 interface
The HFCT-5952 are supplied in the industry standard 2 x 10 DIP style package and are footprint compatible with the SFF MSA. The 2 x 10 transceivers have the same functionality as the 2 x 5 and *Figure 16* shows the common pins between the two packages. The 10 extra pins of the 2 x 10 package provides 3 additional monitoring functions:
- rear facet monitor (P_{MON})
- bias monitor (B_{MON})
- photo detector bias monitor (V_{pdRx})

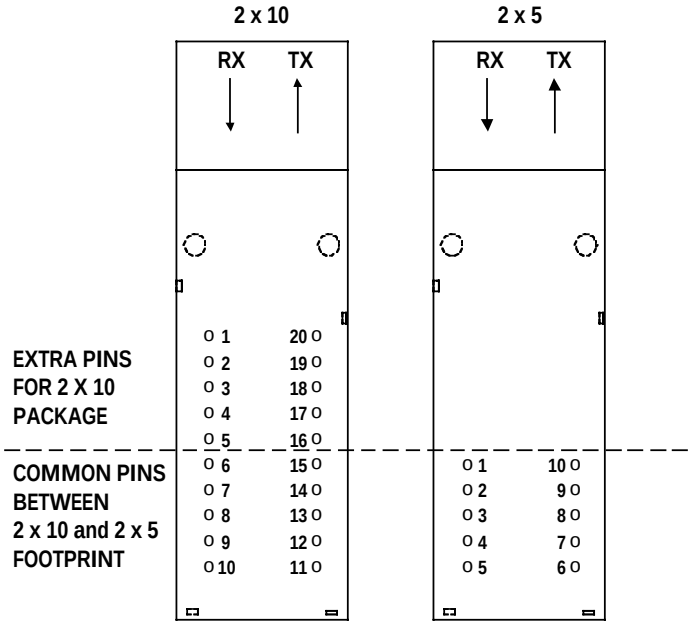


Figure 16. 2 x 10 and 2 x 5 pin out diagrams (top view)

Some applications may not require the use of the additional monitoring functions and the HFCT-5952 may be used in a 2 x 5 configuration. It is recommended to connect the unused pins as follows:

- **Pin 1: photo detector bias.** Must be connected to V_{CC} as shown in *Figure 6* on the data sheet.
- **Pins 2, 3 and 16: V_{EE}.** Connect to ground.
- **Pins 4 and 5:** Do Not Connect.
- **Pins 17, 18, 19 and 20: laser bias and power monitor.** Do Not Connect. Alternatively, these pins can also be left floating.

IBIS Model

An IBIS model, HFCT-5952.ibs, based on measurements is available for the HFCT-5952. The measurements were from a typical HFCT-5952 optical transceiver. The database structure of IBIS allows for a measurement-based model to provide the most accurate representation of a typical transceiver; however, this model does not cover the minimum and maximum corners of the transceiver operation. This model may also be used for the HFCT-5951/5952 as they share similar electronic devices.

The model has been shown to operate in Mentor Graphics ICX software. Downloads are available at **http://www.avagotech.com.**

Recommended Solder and Wash Process

Avago's LC transceivers are compatible with industry standard wave or hand solder processes.

Process Plug

Avago's LC transceivers are supplied with a process plug for protection of the optical ports with the LC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material that will withstand +85°C and a rinse pressure of 110 lb/in^2 .

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the HFCT-5951/5952 fiber-optic transceivers should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha-metals of Jersey City, NJ. Recommended cleaning and degreasing chemicals for the HFCT-5951/5952 are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1. trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N-methylpyrolldone.

Regulatory Compliance

These transceivers are intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. They utilize a carefully designed optical subassembly with a current limiting circuit to guarantee eye-safety. It is intrinsically eye safe and does not require shut down circuitry. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

Normal ESD handling precautions for ESD sensitive devices should be followed while using these transceivers. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas. Additionally, static discharges to the exterior of the equipment chassis containing the transceiver parts must also be considered.

Qualification

These transceivers have been successfully qualified in accordance with the requirements of Bellcore document TA-NWT-000983, under the supervision of Avago Quality and Reliability Engineering.

Recommended References

- HFCT-5951xxx/HFCT-5952xxx data sheet, characterization, reliability
- Application Note 1173: Interfacing to PECL optical transceivers
- Application Note: OC-12 Reference Design using Avago Small Form Factor Transceivers with Vitesse VSC8122 and VSC8141 Multi-rate Chip Set.
- Application Note: OC-12 Reference Design, Quad Serdes for 2 x 10 SFF Transceivers.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

5988-5926EN April 17, 2007

AVAGO TECHNOLOGIES